WHAT IS CLAIMED IS:

1. A zero value-detecting circuit comprising:

an addition means for receiving a 1-bit digital signal produced by encoding an analog signal by delta sigma modulation and taking the sum of said 1-bit digital signals of a given number of samples applied immediately before;

a first decision means for making a decision as to whether said analog signal has a zero value based on the output value from said addition means and for producing a first output signal; and

a second decision means for producing a second output signal indicating that said analog signal assumes a zero value when said first decision means keeps delivering said first signal for a given period of time.

2. The zero value-detecting circuit of claim 1, wherein said number of samples corresponds to N (where N is an integer equal to or greater than 1) times the number of bits of a repeating pattern and appearing in said 1-bit digital signal, correspondingly to said delta sigma modulation, when said analog signal assumes a zero value.

3. The zero value-detecting circuit of claim 1 or 2, wherein said addition means comprises a shift register having stages corresponding in number to said number of samples for which said 1-bit digital signal is received and an adder for summing up values at each stage of said shift register,

and wherein said first decision means produces said first signal when a sum value obtained by said adder corresponds to half of said number of samples.

4. The zero value-detecting circuit of claim 1 or 2, wherein said addition means comprises a shift register having stages corresponding in number to said number of samples for which said 1-bit digital signal is received, a comparison means for comparing the value of the 1-bit digital signal entered into said shift register and the value at the final stage of said shift register and producing a clock signal if they are different, and a counting means of a bit number more than half of said number of samples, said counting means counting UP in response to said clock signal when the 1-bit digital signal entered into said shift register is at a first logical level and counting DOWN when the 1-bit digital signal applied into said shift register is at a second level, and wherein said first decision means produces said first signal when a count value obtained by said counter corresponds to half of said number of samples.